INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
070456-0105	10/573,970
APPLICANT	
Tatsuo HIRAMATSU, et al.	
FILING DATE	GROUP
March 30, 2006	2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 2001/0010074 A1	07-26-2001	NISHIHARA et al.	
		US			
		US			
		US			
		US			
		US			
		US			
		US			
		US			
		US			
		US			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes–Number +– Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		GB 2 333 625 A	07-28-1999	LUCENT TECHNOLOGIES INC.		English (Orig.)	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
/G.G./		European Search Report issued in European Patent Application No. EP 04747279.0-2211/1669868 PCT/JP2004009811, dated February 23, 2009.
/G.G./		Koichiro FURUTA et al., "Spatial-Temporal Mapping of Real Application on a Dynamically Reconfigurable Logic Engine (DRLE) LSI, IEEE 2000 Custom Integrated Circuits Conference, pp.151-154.
/G.G./		Joao M. P. CARDOSO et al., "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XXP Architecture," FPL 2002, LNCS 2438, pp. 864-874.
/G.G./		Joao M. P. CARDOSO et al., "Loop Dissevering: A Technique for Temporally Partitioning Loops in Dynamically Reconfigurable Computing Platforms," 2003 IEEE.
/G.G./		Brad L. HUTCHINGS et al., "Implementation Approached for Reconfigurable Logic Applications," XP-000910926, 1995, P. 419-428.
/G.G./		Steve TRIMBERGER, "Scheduling Designs into a Time-Multiplexed FPGA, XP-000883991, pp. 153-160.

EXAMINER	DATE CONSIDERED
/George Giroux/	11/20/2009

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.